PRACTICAL SYNTHESIS AND ANALYSIS OF ONE RC MODEL OF THE HALF-ORDER CONSTANT PHASE ELEMENT

Plamen NIKOVSKI
University of Food Technologies - Plovdiv, Dept. of Electrical and Electronics Engineering, Engineering Faculty, Plovdiv, Bulgaria
email: plmnn@abv.bg

Keywords: irrational impedance, continued fraction, lattice structure, constant phase element

Abstract: *An approach to the synthesis and realization of a simple RC model of constant phase element of order 1/2 is presented. The main point in the realization of the model is finding the rational approximation of constant phase element impedance function. In this paper, rational approximation is obtained by recursively obtained solutions of the quadratic equation.*
After considering the different structures and influence of tolerances on the accuracy of the impedance function, an eight section lattice cascade was constructed. The deviation between the theoretically and experimentally obtained magnitude and phase characteristics of such a circuit in the frequency interval 0,05÷1MHz did not exceed 1,0 % and 1,2º respectively. Furthermore, it was found that the lattice network performance had impedance close to the expected one but in parallel with a capacity.

1. INTRODUCTION

Numerous detailed approaches have been discussed in the literature for the realizations of constant phase element (CPE) with admittance

$$Y(s) = A.\sqrt{s}\ , \qquad (1)$$

where A is a real number. This is due to the many applications of such network functions in areas like signal processing circuits, robotics, PID controllers, macro-modeling and so forth [1-4]. For analysis, synthesis and implementation of such object, the need often arises for some approximation of $Y(s)$ which yields simple lumped network realizations with known component values. Particularly interesting for the purposes of approximation are rational functions and continued fractions. A real rational function is simply the ratio of two real polynomials:

$$Z_{RF}(s) = \frac{P_\mu(s)}{Q_\nu(s)} = \frac{p_0 + p_1.s + ... + p_\mu.s^\mu}{q_0 + q_1.s + ... + q_k.s^\nu} \qquad (2)$$

where $p_0,p_1,p_2,\ldots p_\mu$, $q_0,q_1,q_2,\ldots q_\nu$, $p_\mu \neq 0$, $q_\nu \neq 0$ are real numbers, μ denotes a non-negative integer that defines the degree of the numerator and ν is a non-negative integer that defines the degree of the denominator.

Another related tool used to find good rational approximations are truncated continued fractions (CF). They are an excellent choice if the practical realization of irrational impedance is needed because:

– CF frequently converges much more rapidly than power series expansions, and converges in a much larger domain in the complex plane [5]. In this case, the final circuit will contain fewer elements, since the required accuracy of approximation can be achieved with low order convergents of the CF;

– Rational approximation in the form of a truncated CF can be directly used to build one-port electrical network with impedance Z_{RF} [6, 7];

– In addition, periodic continued fractions lead to circuits in which the range of values of the elements is less [7, 8]. This is an important advantage because the provision of a large number of elements with different values

(especially when these values are not standard) can be difficult and expensive.

This work presents a simple engineering solution to the problem of implementation of the irrational impedance (1), which has the above advantages.

2. SYNTHESIS BASED ON SOLUTIONS OF QUADRATIC EQUATIONS

Let admittances $Y_a=Y_a(s)$ and $Y_b=Y_b(s)$ are positive real functions [8]:

– Y_a and Y_b are real when s is positive and real;

– $\mathrm{Re}[Y_a(s)]\geq 0$ and $\mathrm{Re}[Y_b(s)]\geq 0$ when $\mathrm{Re}[s]\geq 0$.

It is our intention to present the synthesis of a passive one-port circuit with driving point admittance (DPA) equivalent to their geometrical mean

$$Y=\sqrt{Y_a.Y_b}\ , \qquad (3)$$

where Y is a solution of the equation

$$Y^2=Y_a.Y_b\ . \qquad (4)$$

The equation (4) can be solved in a number of different ways. Let's consider some of them.

Multiplying both sides of (4) by two and after that adding the terms $(Y_a+Y_b).Y$ the equation (5) can be rewritten as it follows:

$$2.Y^2+(Y_a+Y_b).Y=(Y_a+Y_b).Y+2.Y_a.Y_b\ , \qquad (5)$$

$$\big(2.Y+(Y_a+Y_b)\big).Y=(Y_a+Y_b).Y+2.Y_a.Y_b\ ,$$

$$Z=\frac{(Y_a+Y_b).Y+2.Y_a.Y_b}{2.Y+(Y_a+Y_b)}\ ,$$

or:

$$Z=Y_b+\frac{1}{\dfrac{2}{Y_a-Y_b}+\dfrac{1}{Y_b+Y}}\ . \qquad (6)$$

Recursively substituting this expression for Y back into itself yields a continued fraction:

$$Y=Y_a+\cfrac{1}{\dfrac{2}{Y_b-Y_a}+\cfrac{1}{Y_a+Y_a+\cfrac{1}{\dfrac{2}{Y_b-Y_a}+\cfrac{1}{Y_a+\ldots}}}} \qquad (7)$$

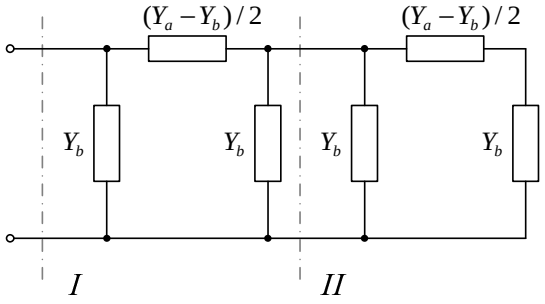

Fig. 1 Circuit of two cascaded Π-sections

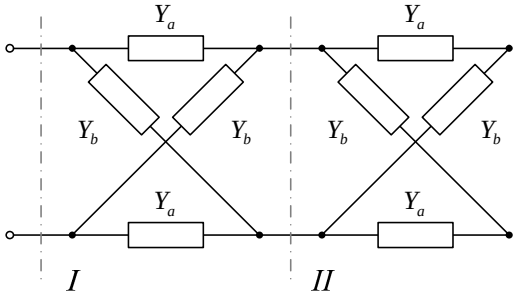

Fig. 2 Circuit of two cascaded lattice sections

Now let's consider the network shown in Fig.1. It presents two cascaded Π-sections. When the right port is an open circuit the driving point admittance $Y_{RF}(s)$ of the entire network can be found easily by considering it in the right-to-left direction:

$$Y_{RF}=Y_b+\cfrac{1}{\dfrac{2}{Y_a-Y_b}+\cfrac{1}{Y_b+Y_b+\cfrac{1}{\dfrac{2}{Y_a-Y_b}+\dfrac{1}{Y_b}}}}\ . \qquad (8)$$

Each Π-section can be transformed into a lattice section using Bartlett's theorem [9] as shown in Fig.2. It is easy to demonstrate that truncation of the continued fraction (7) at a suitable point will result in an approximation of the admittance Y which leads to a finite cascade lattice network. In this case the total number of admittances (TNA) necessary to implement a network of N symmetric lattices will be equivalent to $4N$.

The presented form of a solution of the quadratic equation (4) is not unique. Taking into account (4), from (5) it is obtained:

$$2.Y^2 + (Y_a + Y_b).Y = Y^2 + (Y_a + Y_b).Y + Y_a.Y_b \,, \quad (9)$$

$$\big(2.Y + (Y_a + Y_b)\big).Y = (Y_a + Y).(Y_b + Y) \,,$$

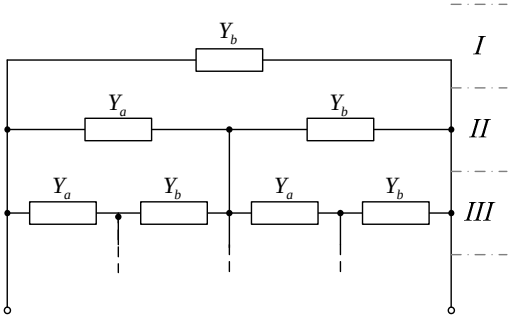

Fig. 3 The generations of mesh network

$$Y = \frac{(Y_a + Y).(Y_b + Y)}{(Y_a + Y) + (Y_b + Y)} \,,$$

$$Y = \frac{1}{\dfrac{1}{(Y_a + Y)} + \dfrac{1}{(Y_b + Y)}} \,. \quad (10)$$

Now we can apply the last equation to itself recursively to obtain the infinite continued fraction in the limit.

$$Y = \cfrac{1}{\cfrac{1}{Y_a + \cfrac{1}{\cfrac{1}{Y_a + \ldots} + \cfrac{1}{Y_b + \ldots}}}} + \cfrac{1}{Y_b + \cfrac{1}{\cfrac{1}{Y_a + \ldots} + \cfrac{1}{Y_b + \ldots}}} \,. \quad (11)$$

The equation (11) leads to a circuit shown in Fig.3.

The network begins with a branch of admittances $Y_a(s)$ and $Y_b(s)$ in series which build the first generation.

Similar branch is connected in parallel to $Y_a(s)$ and $Y_b(s)$ forming the next generation.

This process is repeated and the number of the simple loops in the network has increased. In this case the DPA of an *M*-generational network is consisted of 2^{M+1}-2 separate impedances.

3. PROPERTIES OF LATTICE AND MESH STRUCTURE NETWORK REALIZATION

The expressions:

$$Y(s) = A.\sqrt{s} \quad (12)$$

and:

$$Y(s) = \frac{1}{A.\sqrt{s}} \quad (13)$$

represent some of the simplest irrational admittances.

According to equation (3) infinite lattice or infinite mesh structure network composed of resistances Y_a=1/*R* and capacitors Y_b=*s*. *C* will have DPA as in (12) where:

$$A = \sqrt{\frac{C}{R}} \,. \quad (14)$$

Unfortunately, real circuits contain a finite number of elements. When we are looking for proper practical realization it's important to know:

– the accuracy of approximation with a definite number of admittances (or components);

– the sensitivity of the network to changes of the admittance parameters.

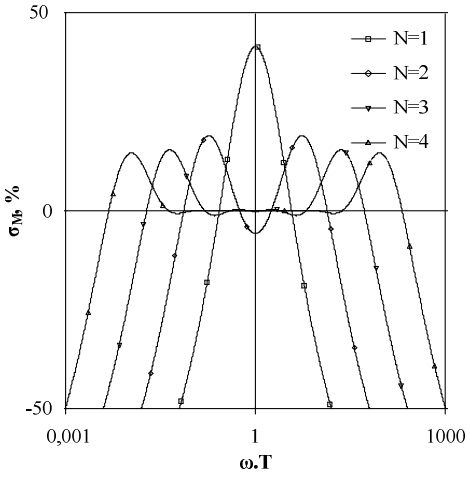

Fig. 4 Magnitude error refers to specific realization of the lattice network

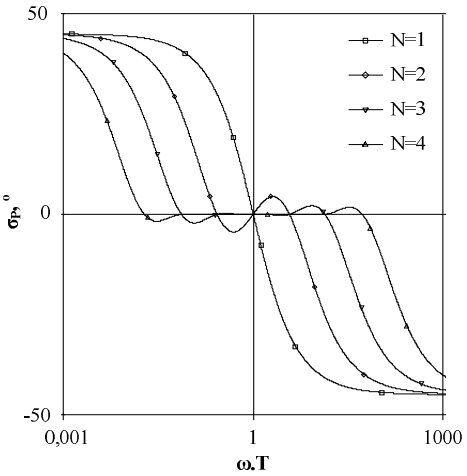

Fig. 5 Phase error refers to specific realization of the lattice network

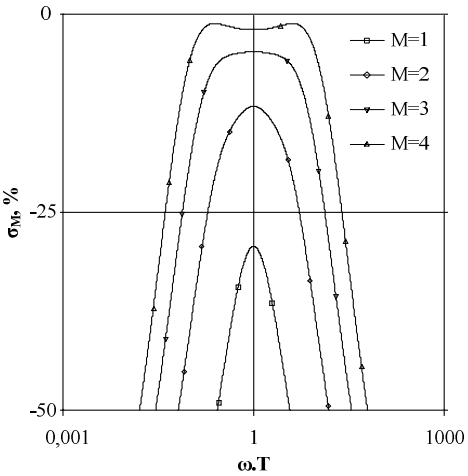

Fig. 6 Magnitude error refers to specific realization of the mesh network

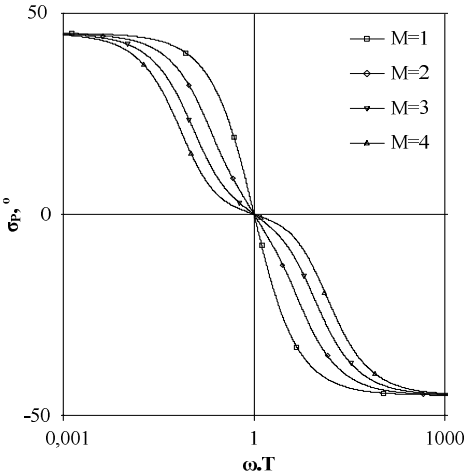

Fig. 7 Phase error refers to specific realization of the mesh network

Increasing the number of sections in the lattice structure or the number of generations in the mesh structure will result in a DPA more close to (12). But this process is not the same for both structures. In Fig.4-7 are depicted the magnitude error

$$\sigma_M = \frac{|Y_{RF}| - |Y|}{|Y|}.100,\% \qquad (15)$$

and the phase error

$$\sigma_P = \angle Y_{RF} - \angle Y \qquad (16)$$

of some specific realization. These results were obtained using the PSpice. The maximum absolute value of σ_M and σ_P:

$$\sigma'_M = \max|\sigma_M| \qquad (17)$$

$$\sigma'_P = \max|\sigma_P| \qquad (18)$$

in the frequency interval $0{,}1 \le \omega.T \le 10$, $T=R.C$ is given in Table 1. It can be seen that the considered networks have the following features:

– when TNA does not exceed 32, the number of possible realizations is eight for a lattice and four for a mesh network;

– when TNA is equal to eight or more, the lattice network achieves better σ'_M and σ'_P than the mesh network at a smaller number of elements.

Manufacturing tolerances of the resistors and capacitors also affect the accuracy of realization. Monte Carlo analysis is perhaps the most well-known method for evaluating this influence. It is a purely statistical method in which the tolerance values are varied by a random algorithm over a number of simulation runs. Using PSpice Monte Carlo analysis the maximum value of σ'_M and σ'_P for a set of 300 runs is obtained. The results for the different tolerances are listed in Table 1-4.

Table 1 Magnitude and phase error when the circuit elements have a nominal value

σ'_M %	σ'_P °	*Type*	TNA
68.5	39.3	Mesh	2
41.4	39.3	Lattice	4
39.8	31.5	Mesh	6
18.9	19.5	Lattice	8
18.4	22.8	Mesh	14

15.0	3.16	Lattice	12
5.64	15.4	Mesh	30
5.56	2.14	Lattice	16
0.95	1.52	Lattice	20
0.83	0.44	Lattice	24
0.47	0.12	Lattice	28
0.09	0.10	Lattice	32

Table 2. Magnitude and phase error when the circuit elements have a tolerance of 2%

σ'_M %	σ'_P °	Type	TNA
69.2	39.5	Mesh	2
43.31	39.5	Lattice	4
40.9	31.9	Mesh	6
20.4	20.1	Lattice	8
19.7	23.4	Mesh	14
16.6	3.7	Lattice	12
7.11	16	Mesh	30
7.01	2.47	Lattice	16
2.16	1.92	Lattice	20
2.06	0.755	Lattice	24
1.9	0.523	Lattice	28
1.73	0.419	Lattice	32

Table 3. Magnitude and phase error when the circuit elements have a tolerance of 1%

σ'_M %	σ'_P °	Type	TNA
68.9	39.4	Mesh	2
42.4	39.4	Lattice	4
40.4	31.7	Mesh	6
19.7	19.8	Lattice	8
18.8	23.1	Mesh	14
15.7	3.43	Lattice	12
6.33	15.7	Mesh	30
6.25	2.31	Lattice	16
1.71	1.55	Lattice	20
1.12	0.652	Lattice	24
1.01	0.285	Lattice	28
0.965	0.294	Lattice	32

Table 4. Magnitude and phase error when the circuit elements have a tolerance of 0,5%

σ'_M %	σ'_P °	Type	TNA
68.7	39.3	Mesh	2
41.9	39.3	Lattice	4
40.1	31.6	Mesh	6
19.7	19.3	Lattice	8
18.8	22.9	Mesh	14
15.4	3.29	Lattice	12
5.96	15.6	Mesh	30
5.9	2.22	Lattice	16
1.32	1.62	Lattice	20
1.19	0.55	Lattice	24
0.82	0.21	Lattice	28
0.45	0.18	Lattice	32

Following previous recommendations the circuit of eight lattice section has been implemented.

The resistors and capacitors have a nominal value of 4,3kΩ and 68pF respectively, and a tolerance of 0,5%.

The input impedance of the circuit is measured by means of the impedance analyzer Agilent 4294A in a frequency interval 0,05÷1MHz.

As shown in Fig.8 and Fig.9 the experimentally obtained errors σ'_M and σ'_P increase with the increase in frequency and they are several times greater than the errors in Table 4. This is due to the frequency-dependent effects in the real resistors and capacitors, together with the strain immittance in the circuit performance.

These phenomena are complex and difficult to predict. Taking into account that $\sigma_M>0$ and $\sigma_P>0$, we fit the experimental data to a simple model composed of admittance (12) and capacitor $C_i\approx1,3$pF in parallel. The value of C_i is found by minimizing the functional

$$\psi = \sum_i \left[\left(\frac{\sigma'_M(f_i)}{0,45} \right)^2 + \left(\frac{\sigma'_P(f_i)}{0,18} \right)^2 \right] \quad (19)$$

in the given frequency interval. If the admittance of C_i is subtracted from the input admittance of the circuit, the errors (17) and (18) will be close to the values in Table 4.

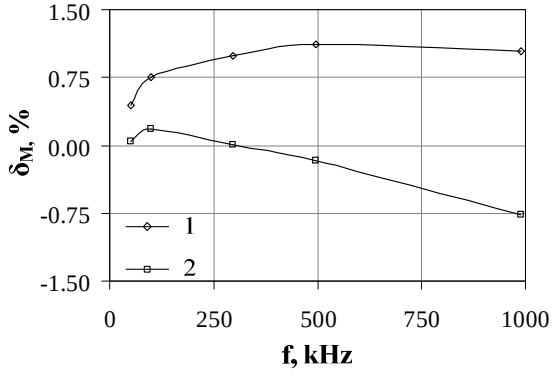

Fig. 8 Curves 1 and 2 represent the magnitude error of the circuit realization before and after the admittance of C_i is subtracted from the Y(s)

4. EXPERIMENTAL RESULTS

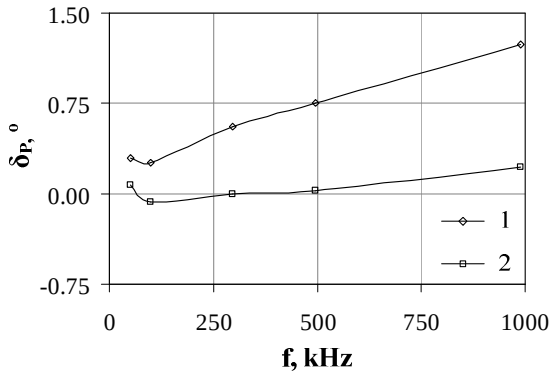

Fig. 9 Curves 1 and 2 represent the phase error of the circuit realization before and after the impedance of C_i is subtracted from the Y(s)

5. CONCLUSION

Papers [10, 11] describe synthesis of irrational admittance $A.s^{\alpha}$, $0 \leq \alpha \leq 1$ of arbitrary order, which is used to create a model for numerical simulation in PSpice.

Unfortunately, such a model is not suitable for physical implementation because the elements of the circuit have very different values. The lattice circuit and the mesh circuit are constructed of identical resistors and capacitors. Both circuits present a solution of the same equation but have different properties.

The lattice circuit can be implemented in more different variants and when the number of elements is equal to eight or more, it offers better accuracy.

Experimental data showed that in the frequency interval 0,05 ÷ 1 MHz the lattice circuit realization has an input admittance close to the irrational admittance $A.s^{0,5}$ in parallel with some capacitor C_i. The impact of C_i can be ignored if it does not need an accuracy presentation (in this case the magnitude and phase error do not exceed 1,0% and 1,2º respectively).

The results in this work were successfully used to study the effect that a phase constant element has on charge transfer processes in capacitive transducers and validation of measurement methods suitable for this case [12, 13].

6. REFERENCES

[1]. Radwan, A., Soliman A., Elwakil A., "*First order filters generalized to the fractional domain*", Journal of Circuits Systems & Computers, Vol. 17, pp. 55-66, 2008.

[2] Krishna, B., Reddy K., "*Active and passive realization of fractance device of order 1/2*", Journal of Active and Passive Electronic Components, Vol. 2008, p.5, 2008.

[3] Podlubny I., "*Fractional-order systems and fractional-order controllers*", Slovak Academy of Sciences, Slovakia, p.21, 1994.

[4] Soulier F., Lagonotte, P., "*Modeling distributed parameter systems with discrete element networks*", Proceedings of 15th International Symposium on the Mathematical Theory of Networks and Systems, p.7, 2002.

[5] Press W., Teukolsky S., Vetterling W., Flannery B., "*Numerical Recipes in C: The Art of Scientific Computing*", Second Edition, Cambridge University Press, p.994, 2002.

[6] Sudhakar A., Palli S., "*Circuits and Networks*", Tata McGraw-Hill Education, p.965,2006.

[7] Chitode J., Jalnekar Dr., "*Network Analysis and Synthesis*", Technical Publications, p.853, 2007.

[8] Wing O., "*Classical Circuit Theory*", Springer, p.296, 2008.

[9] Iyer T., "*Circuit theory*", McGraw-Hill, p.520, 2006.

[10] Nikovski Pl., Katrandziev N., "*Modelling of phase-constant element in PSpice environment*", Scientific conference with international participation – Food science, Engineering and Technologies, pp. 430-435, 2009.

[11] Nikovski Pl., "Improving the metrological characteristics of capacitive charge transfer transducers in the presence of constant phase element in the input", PhD thesis, Technical University, p.128, 2011.

[12] Nikovski Pl., "*A transfer function of a capacitive transducer in the presence of a phase constant element*", Engineering Sciences, No.3, pp.12-21, 2010.

[13] Nikovski Pl., Maslinkov I., "*Analysis of an equivalent CCPE connection diagram of the one-port circuit by square-wave voltage*", International Scientific and Applied Science Conference Electronics, pp.197-199, 2009.